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10/728,962	12/08/2003	Deborah T. Marr	2207/794102	9038

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KENYON & KENYON LLP
1500 K STREET N.W.
SUITE 700
WASHINGTON, DC 20005

EXAMINER	
MOLL, JESSE R	
ART UNIT	**PAPER NUMBER**
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/728,962	MARR ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 21-28 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

> Claims to computer-related inventions that are clearly nonstatutory fall into the same general categories as nonstatutory claims in other arts, namely natural phenomena such as magnetism, and abstract ideas or laws of nature which constitute "descriptive material." Abstract ideas, Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759, or the mere manipulation of abstract ideas, Schrader, 22 F.3d at 292-93, 30 USPQ2d at 1457-58, are not patentable. Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data (See MPEP section 2106, IV, B, i).

3. Claim 21 comprises steps of determining, pausing, and resuming. The steps are just an abstract idea. The claim does not provide practical application that produces a useful, tangible and concrete result. Therefore, the claim is non-statutory. Similar problems exist in the other claims 22-25 since the additional limitations claimed therein do not provide practical application that produces a useful, tangible and concrete result.

Note that the pausing and resuming of "processing" is just an abstract idea. The limitations do not require a useful, tangible and concrete result to occur. The limitation "processing" includes merely moving the instructions. The limitations merely manipulate movement of data (pausing and resuming the movement of data). Examiner suggests changing the limitation "processing" to "execution" to impose functionality on the instructions.

Claim 26 comprises steps of determining, initiating, and pausing. The steps are just an abstract idea. The claim do not provide practical application that produces a useful, tangible and concrete result. Therefore, the claim is non-statutory. Similar problems exist in the other claims 27 and 28 since the additional limitations claimed therein do not provide practical application that produces a useful, tangible and concrete result.

Similar problems exist as in Claim 21. Examiner suggests changing "processing" on lines 5 and 6 to "execution" and adding a limitation to start execution after said counter reaches said predetermined value.

Withdrawn Rejections

4. Applicant, via amendment, has overcome the rejection of Claims 21-25 under 35 U.S.C. 112 second paragraph. The rejection has been respectfully withdrawn.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 21-25, and 29-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Emer et al. (USA 6,493,741) (Herein referred as Emer et al.).

7. Referring to claim 21, Emer et al. discloses, as claimed, comprising the steps of: determining whether a first instruction (QUIESCE 117, Fig. 2, and Col. 5, lines 34-35) for a first thread is an instruction of a first type (the type having QUIESCE operation) at a pipeline stage of a processor (see Col. 4, lines 15-18 regarding the program instruction propagating into the pipeline); pausing processing of instructions of said first thread (Col. 5, lines 35-36, and Col. 7, lines 33-36 regarding halting the execution of the thread) at said pipeline stage for a period of time (note the Emer et al.'s system also uses a timer 107, see Fig. 8, Col. 5, lines 63-64, and Col. 6, lines 9-11) if said first instruction is of a first type (the type having QUIESCE operation) while processing instructions from a second thread (see Col. 4, lines 32-34 regarding allowing other executing

programs to utilize available resources when the first thread is paused) at said pipeline stage (note the instructions in the second thread can be selectively fetched (by the thread multiplexer 353) and arranged in the pipeline see Fig. 4;

Further note that instructions for that thread are paused in all pipeline stages. The processor idles that thread in response to the QUIESCE instruction);

and resuming processing (see Col. 9, lines 17-21 regarding resuming the processing) of instruction of said first thread in response to the determining operation at said pipeline stage (The thread is paused in response to the QUIESCE instruction).

Note claim 21 recites the corresponding the limitations of claim 29, as set forth above. Note Emer et al.'s CPU certainly comprises a decode unit therein; and an instruction is certainly decoded into several microinstructions in the Emer et al.'s system to determine whether a first instruction (QUIESCE 117, Fig. 2, and Col. 5, lines 34-35) of a first thread is an instruction of a first type (the type having QUIESCE operation).

8. As to claim 22, Emer et al. certainly taught: decoding said first instruction (QUIESCE 117, Fig. 2, Col. 5, lines 34- 35) into a first microinstruction and a second microinstruction (since a decode unit certainly exists in the Emer et al.'s CPU; and an instruction is certainly decoded into several microinstructions in the Emer et al.'s system). Note the limitations of claim 22, as set forth above, comprise the claimed limitations described in claim 30.

9. As to claim 23, Emer et al. explicitly taught: said first microinstruction causes a value (inside the watch flag indication 105, see Col. 5, lines 59-60) to be stored in memory (the register of watch flag indication 105, Fig. 2) for said first thread. Note the limitations of claim 23, as set forth above, comprise the claimed limitations described in claim 31.

10. Referring to claim 24, Emer et al. explicitly taught: processing said microinstruction for execution when said value stored in memory is reset (see Col. 7, lines 37-38, regarding when the watch flag is cleared). Note the limitations of claim 24, as set forth above, comprise the claimed limitations described in claim 32.

11. Referring to claim 25, Emer et al. explicitly taught: said value stored in memory value (watch flag 105) is reset when said first microinstruction is retired. Note "said first microinstruction is retired" is given broadest reasonable interpretation as the QUIESCE instruction (Fig. 2, Col. 5, line 34-35) is terminated by an interrupt as mentioned in Col. 9, lines 18-20. Note claim 33 recites the similar limitations as set forth. The interrupt servicing routine (see Col. 9, lines 18-20) is best reasonably and broadly interpreted as a retire unit as claimed.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 26-28, and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emer et al.

14. Referring to claims 26-28, Emer et al. discloses the claimed invention except for: initiating a counter; and pausing processing of instructions of said first thread at a pipeline stage of a processor until said counter reaches a predetermined value while processing instructions for a second thread at said pipeline stage; and the first instruction including an operand and the initiating including loading the counter with the operand (in Claims 26-28 and claims 34-36 recite the similar limitations.)

However, Emer et al., as set forth above, using a timer (107, Fig. 2) to pause processing of instructions of said first thread (see Fig. 8, Col. 5, lines 63-64, and Col. 6, lines 9-11).

Further, using a counter to control the time during a process in a computer system; and loading the counter with the operand to flexibly control the length of time are well known in the art.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Emer et al.'s system to comprise initiating a counter; pausing processing of instructions of said first thread at a pipeline stage of a processor until said counter reaches a predetermined value while processing instructions for a second thread at said pipeline stage; and the first instruction including an operand and the initiating including loading the counter with the operand since using the counter is just an alternative way to flexibly control the length of time as comparing with the timer used in the Emer et al.'s system.

Response to Arguments

15. Applicant's arguments filed 6 November 2006 have been fully considered but they are not persuasive.

16. With respect to arguments regarding the rejection under 35 U.S.C. 101, a detailed analysis is given above.

17. Applicant states:

> In the Response to Arguments section, the Office Action provides new arguments as to the applicability of Emer to the pending claims. Applicants in their previous Amendment pointed out that in Emer, the entire thread processing unit is quiesced. If such a TPU includes pipeline stages (though none are described in Emer), then none of those pipeline stages would be processing instructions from a second thread as called for in claims 21 and 26.

Examiner disagrees. Emer discusses a pipeline (see col. 4, lines 12-14), therefore there must be pipeline stages. Claims 21 and 26 merely require instructions to be processed, there is no limitation as to what processes them. Further, claim 29 states that "instructions from a second thread **can** be processed". This does not require instructions from a second thread to be processed, but merely makes the processing optional.

18. Applicant states:

> The Office Action points to Col. 5, lines 35-36 and Col. 7, lines 33-36 as describing pausing instruction of the first thread. The text at Col. 5 states that the QUIESCE instruction is "a request to quiesce, or halt, execution of the thread executing the QUIESCE." The text at Col. 7 indicates that when the QUIESCE instruction is executed, the TPU ceases executing instructions from the program. The Office Action further states that the Emer system includes a timer 107 as described at Col. 5, lines 63-64 and Col. 6, lines 9-11. As indicated by the text, the timer is started upon execution of the QUIESCE instruction.
>
> The Office Action further points to Col. 4, lines 32-34 as allowing other executing programs to utilize available resources when the first thread is paused. The text of this section says "[h]alting execution of, or quiescing, the program results in a reduction of power consumption, and allows other executing programs to utilize available resources. The Office Action points to multiplexor 353 in Fig. 4 as providing a specific example of this. Claim 21 recites determining whether a first instruction for a first thread is an instruction of a first type at a pipeline stage of a processor and pausing processing of instructions of the first thread at said pipeline stage. As seen in Fig. 4, both of these operations are not being performed. There is no determination made at a pipeline stage that an instruction is of a first type and then pausing processing of instructions at said pipeline stage. In Emer, a QUIESCE instruction has been previously executed resulting in a quiesce state that is used for the Mapper operation shown in Fig. 4. Instructions after the QUIESCE instruction presumably were passed through multiplexor 353 before the QUIESCE instruction was executed. Accordingly, if a determination is made in Emer, it would be done at the execution unit of the processor, and other instructions already in the pipeline would continue to be processed. Claim 26, includes similar limitations to claim 21.

Examiner disagrees. Inherently, in a pipeline processor, any action must be done in a pipeline stage. If execution of a first thread is halted, the second thread would percolate through the pipeline. The first thread is paused (forced to not execute) in response to a QUIESCE instruction. Certaintly, the first thread would not be executing in any of the pipeline stages (since it is stopped from percolating through the pipeline). Thus, the first thread is paused in all pipeline stages, including the pipeline stage for determining a QUIESCE instruction. Further, the term "stage" is a very broad term and the entire processor can be considered a stage. The definition of "stage" according to Dictionary.com Unabridged (v 1.1) is "a single step or degree in a process; a particular phase, period, position, etc., in a process, development, or series". Using this definition, a pipeline stage, is merely a step in the execution.

19. Applicant states:

> As to claims 29 and 34, these claims refer to a decode unit that is to determine whether a first instruction is of a first type and is to pause processing of instructions. In response to this argument, the Office Action points to Emer's CPU including a decode unit and cites the language of Col. 5, lines 34-35, which describes the QUIESCE instruction as one that when executed halts execution of instructions in a thread. Applicants argument is that claims 29 and 34 refer to a decode unit having recited features, and that Emer does not teach or describe a decode unit having those features. The words "decode" or "decoder" do not appear in Emer. Even assuming that the CPU of Emer includes a decoder, since there is no mention of a decoder in Emer, it cannot be said that Emer teaches or suggest a decoder or decode unit that includes the features recited in the claims.

Examiner disagrees. Although Emer does not expressly speak of a "decoder", the functionality of the claimed decoder (Claims 29 and 34) is

described. Inherently, there must be a physical structure to perform these actions. The definition of "decoder" according to Dictionary.com Unabridged (v 1.1) is "a circuit designed to produce a single output when actuated by a certain combination of inputs." Any structure performing the actions of Claims 29 and 34 can be considered a decoder. Anticipation does not require word for word disclosure of the claim.

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is

(571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571)272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 1/22/07

DONALD SPARKS
SUPERVISORY PATENT EXAMINER